09/187197 (Spec.)

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 to Fig.6 show the prior art shallow trench isolation method of a semiconductor wafer.

Fig.7 to Fig.11 show a method of forming dummies according to the present invention.

Fig.12 to Fig.14 show another method of forming dummies according to the present invention.

Fig.15 to Fig.~~16~~ 17 show a shallow trench isolation method of a semiconductor wafer according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention relates to a shallow trench isolation method of a semiconductor wafer. The method involves first separating large shallow trenches into multiple trenches of smaller width by generating several dummies followed by filling the shallow trenches with dielectric material. Please refer to Fig.7 to Fig.11. Fig.7 to Fig.11 show a method of forming dummies according to the present invention. As shown in Fig.7, a semiconductor wafer 30 comprises a Si substrate 34, a pad oxide layer 36 composed of SiO_2 formed over the Si substrate 34, and a pad nitride layer 38 composed of Si_3N_4 deposited over the pad oxide layer 36. First, shallow isolation trenches are formed on the semiconductor wafer 30. Shallow trenches with widths greater than about 2 μm are used for generating dummies. A plurality of photoresists 32 are applied on the surface of the semiconductor wafer 30 to determine the positions of the shallow trenches by performing photolithography and etching. Then, the surface of the